Wordmaker

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Constructional details by Glenn Rogers and Peter Kershaw

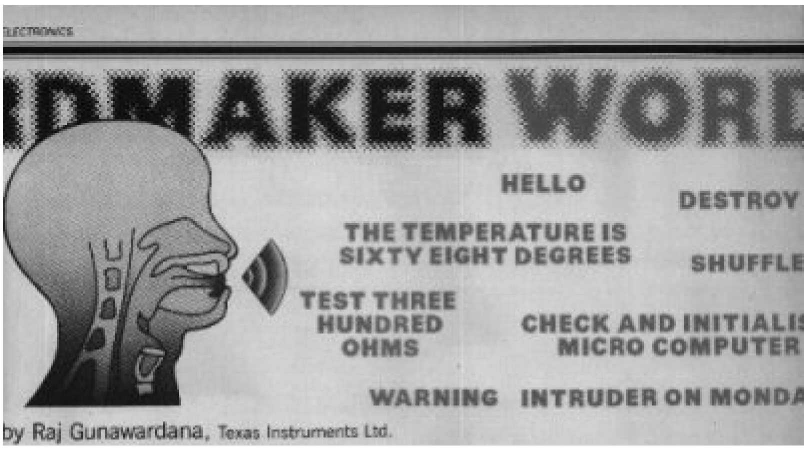
E and MM brings you the first majar Solid State Speech project for under 100 UK pounds
Promises to have a dramatic impact on state-of-the-art electronics - now, and for generations to come
Complex talking library of over 200 words with further expansion space
Easy interfacing to a microcomputer through a few lines of BASIC
Pitch control has exciting electronic music applications

x

Wordmaker

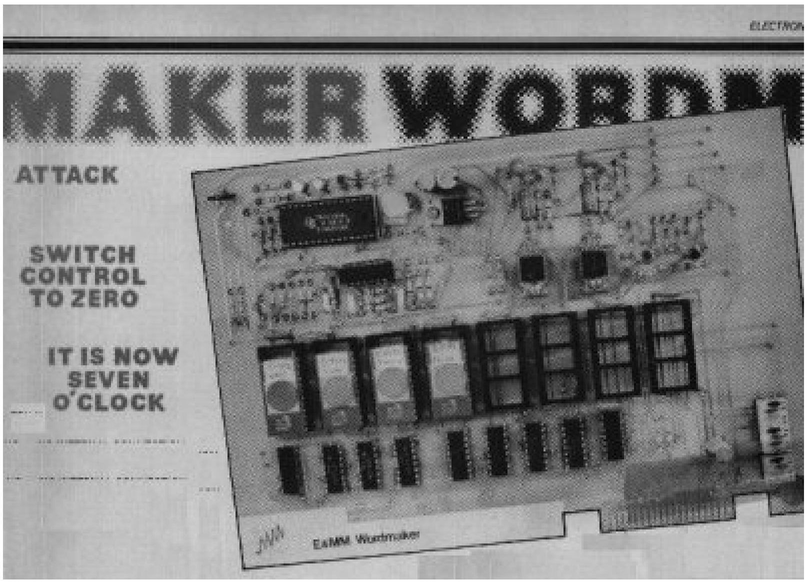
For some ten years Texas Instruments have been developing solid state speech technology with the result that speech can now be produced which faithfully preserves the character of the spoken voice including intonation, accent, dialect, and pitch. Linked to a microcomputer, words can be strung together to make complete phrases and sentences so that voice communication between 'computer' and human becomes possible.

Wordmaker



The uses of this project are far reaching and will be of benefit to almost anyone who uses it. The carefully selected word library has many applications in the home and industry, for telephone, burglar alarms, conversations, messages, games, electronic terms, studio control speaking clock, temperature indication, calendar, business coding, factory announcements, and accountancy.
This month we shall present the complete building project which can be purchased as a kit and explain how to interface the WORDMAKER board to a microcomputer. Possible interface circuits are included and BASIC programs are also given. It has already been fully tested on the Sharp MZ-80K and Tangerine systems. Further details are provided later for other popular micros and we shall be following this article with additional information on the processes of speech synthesis employed, and readers' ideas for interfacing and use will be welcomed.
The E and MM WORDMAKER Speech Synthesiser is based on the Texas Instruments Voice Synthesis Processor (VSP). This card can be interfaced to any computer system or used as an independent unit. The card comprises the Texas TMS 5100 Voice Synthesis Processor; a memory bank containing the vocabulary and an onboard amplifier.

VSP card

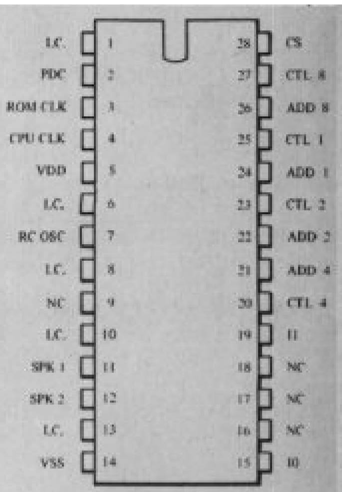


The synthesis method used is called Linear Predictive Coding (LPC). This is a technique developed by Texas which minimises the amount of storage needed for each word. Human speech, like most communication signals, contains a large proportion of redundant information. LPC involves looking at the complete word as a binary data string and removing any redundant data. The coding is then tested to check that the word is spoken satisfactorily. The TMS 5100 contains a 10pole digital filter which synthesises the voice; the filter is controlled by the LPC data. For each word sample, the length of the data string written to the TMS 5100 may vary from 4 to 49 bits. The device, therefore, requires quite a high level of 'intelligence'.

The Heart of the System-TMS 5100

The TMS 5100 has five control lines. The command is set up on the CTL lines and executed by toggling the command clock line, PDC. Table 1 shows the complete list of commands and Figure 1 gives the pin configuration of the IC.

Figure 1: TMS 5100 pin details
Table 1: The TMS 5100 VSP Command Summary



NC — NO INTERNAL CONNECTION
IC — INTERNAL CONNECTION
CS — CHIP SELECT
CTL (1,2,4,8) — CONTROL LINE (1,2,4,8)
PDC — PROCESSOR DATA CLOCK
ADD (1,2,4,8) — ADDRESS/DATA (LINE) TO ROM
I (0,1) — CONTROL LINES TO ROM
CPU CLK — CONTROLLER SYNCHRONISATION (320kHz) CLOCK
ROM CLK — 5100 O/P TO V/S ROM (160kHz)
SP (1,2) — DIFFERENTIAL AUDIO OUTPUT

Figure 1. TMS 5100 pin details.

INSTRUCTION NAME	CTL PINS 8	4	2	1	TOGGLES OF PDC REQUIRED
RESET	0	0	0	X	1 (3 ON POWER UP)
LOAD ADDRESS	0	0	1	X	2
READ and BRANCH	1	1	0	X	1
SPEAK	1	0	1	X	1
TEST BUSY	1	1	1	X	3
READ BIT	1	0	0	X	1
OUTPUT	0	1	0	X	3

X – DON'T CARE

Table 1. The TMS 5100 VSP Command Summary.

Load Address Command: This command causes the VSP to accept a subsequent nibble (4-bits) of data set up on CTL lines as a speech address segment which is transferred to voice synthesis (V/S) ROM address registers. Read and Branch: This instructs the VSP to set up appropriate control signals to the V/S ROM, causing it to update its address registers with the contents of the currently addressed pair of bytes.

Speak: On receiving this command, the VSP takes over the control of the V/S ROM and generates pulses on its l/O line to fetch bit serial data from ROM and commences speech. Pulses on the I/O line occur in bursts of a frame interval of twentyfive milliseconds. The number of pulses in any one frame varies from 4 to 49, depending on the data. The timing of I/O pulses for a maximum length of 49 bits, is shown in Figure 2. Details of the data structure will be discussed in a future article.

Figure 2: IO Pulse and Data input to TMS 5100 in Talk mode

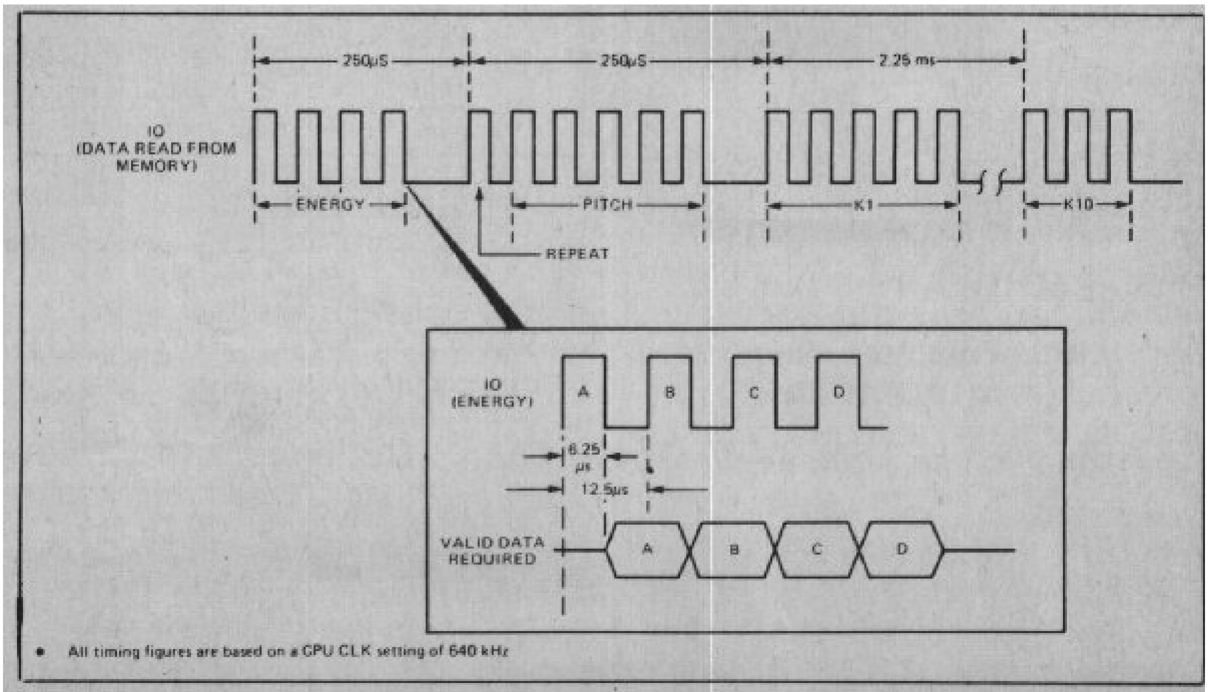


Figure 2. IO Pulse and data input to TMS 5100 in Talk mode.

Test Busy: This command permits the controller to access the TALK STATUS LATCH of the VSR In operation the command is first set up on CTL lines and the PDC line toggled once. A subsequent toggle of the PDC line enables the Talk Status to be output to CTL1 line. The Talk Status will be high during the execution of speech generation and will be set low on an END or PHRASE code being' encountered. A third toggle of the PDC line is required to return the VSP to a state of accepting new commands.

Read Bit: This command causes the VSP to generate a single pulse on the I/O line and thus read a single bit of data. Each data read is input via the ADD8 line to 4-bit shift register in the VSP. Hence four consecutive read operations are required to completely update the shift register contents.

Output: On receiving this command the VSP is initialised into outputting its buffer contents to the CTL lines. A second PDC toggle enables the CTL output buffers and a third is required to return the VSP to the command mode. The output commamd coupled with Read Bit thus allows the controller to access auxillary data stored in the V/S ROM.

Reset: This command is used to establish known initial conditions in the internal circuitry of the VSP in readiness for a following sequence of commands. Since, the CTL lines convey data as well as commands to the VSP, when previous conditions are not known, it is possible that a command can be conveyed as data. Hence, it is necessary toggle PDC at least three times whilst maintaining the Reset command on CTL lines, to ensure correct synchronisation of subsequent commands. Reset can be used in the middle of speech to stop VSP execution. In the circuit design discussed in this article only the Reset, Test Busy and Speak commands are used.

Interfacing the VSP Design Considerations

The following requirements have been considered in interfacing the TMS 5100 to a microcomputer to operate as a speech peripheral:

(1) SPEECH DATA MEMORY should have means of serial data output and an autoincrementing address register for sequential data access.

(2) SPEECH DATA ADDRESS should be presetable from the host processor to define current enunciation required.

(3) THE CONTROL INTERFACE should be consistent with device specifications (of TMS 5100)
(4) SIGNAL LEVELS to and from the controller should be TTL compatible.

As far as speech data memory is concerned, two approaches can be made in implementation:
(1) Speech data can be stored externally to the processor in nonvolatile memory for stand alone operation.
(2) Speech data can be supplied from within the processor with synchronisation to suit the TMS 5100 timing (see Figure 2).

Figure 3: VSP interface

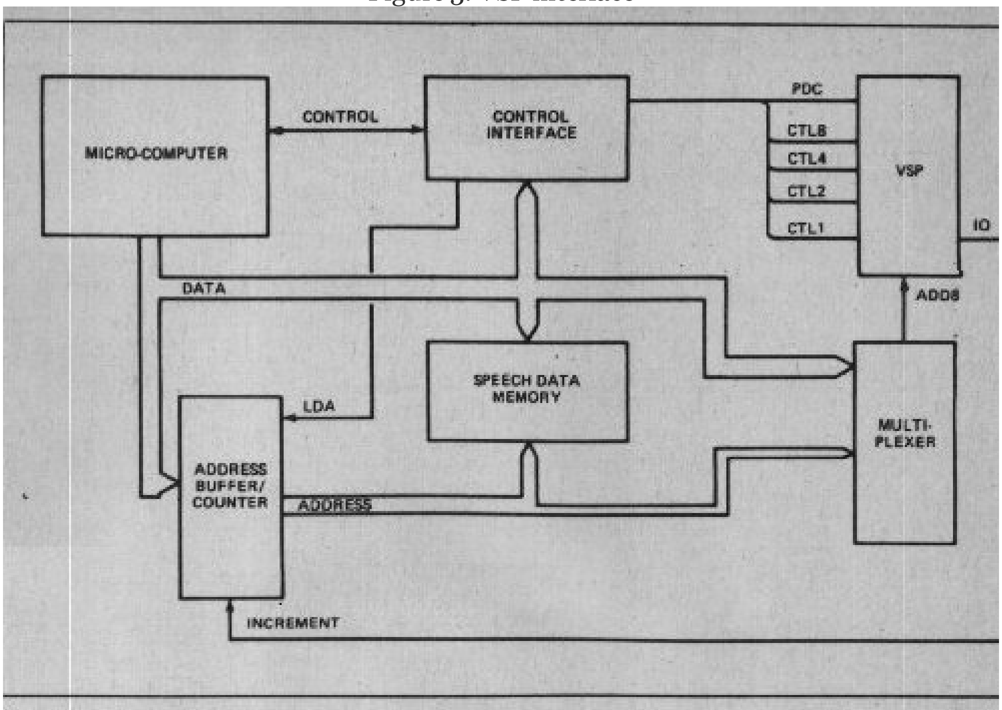


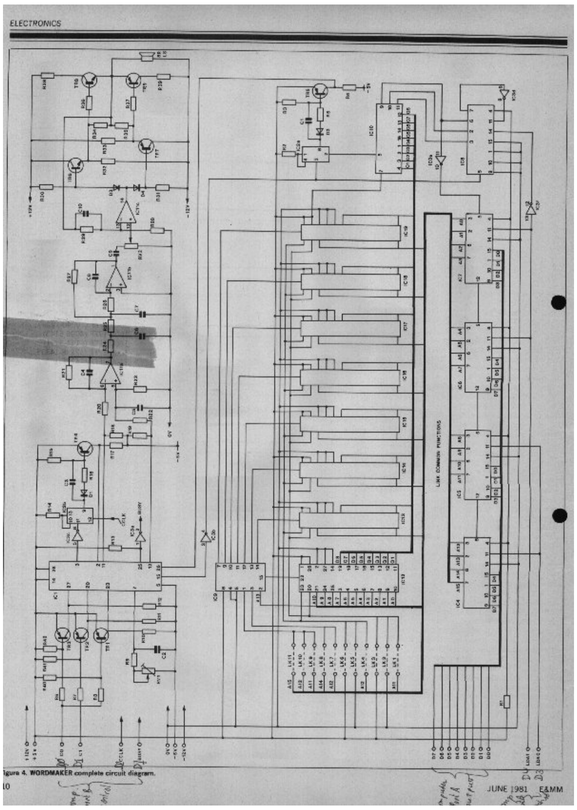
Figure 3. VSP interface.

The circuit discussed in this article takes the first approach, to achieve stand alone operation. Figure 3 shows how the VSP could be interfaced toa microcomputer by implementing a direct data path between the address counter (and the controller, instead of via the TMS 5100 CTL lines. This feature avoids the neeed to decode various commands (e.g. Load Address), to maintain a record of command sequences and to build up the contents of the address registers, one nibble at a time.
Speech data memory can, in theory, either be non-volatile or Random Access Memory (RAM). If memory comprises RAM, it would be possible to 'overlay' speech code read out from a slow bulk storage peripheral such as floppy disc or cassette tape. The circuit discussed in this article, however, uses a choice of EPROM types for speech data storage.

Practical Implementation

Figure 4 shows a practical circuit designed in accordance with the architecture discussed. The circuit is designed to be driven from a byte oriented bus and requires a number of control bits to clock data and to monitor VSP busy conditions. Once commanded to TALK, the circuit will operate independently of the processor to generate a single utterance. Concatenation of such utterances has to be carried out by the host processor.

Figure 4: Wordmaker complete circuit diagram



The Control Interface. The control interface comprises four lines named C0, C1, CCLK and BUSY. C0 and C1 are used to set up three commands on CTL2, CTL4 and CTL8 lines, as shown in Table 2.Transistors TR1,TR2 and TR3 are used to convert TTL levels to drive voltages suited to the TMS 5100. CCLK is used to clock commands set up on C0 and C1 lines into the VSP. The VSP clock line, PDC, has to change synchronously with the VSP ROM clock line. This is achieved by the use of lC2b as a synchroniser. The CCLK line should therefore be held high for a minimum duration, of 6.25 microseconds to guarantee that a command would be accepted by the VSP. The busy line can be used in one of two ways to monitor the end of an utterance.. During speech and when the CTL1 line is in a disabled state, the BUSY line will be low, producing a high level only when CTL1 is enabled and subsequent to encountering an END OF PHRASE code. Hence, the host processor can be made to monitor the BUSY line until a high level is detected. Alternatively, more efficient use of the, host processor can be achieved by using the positive going edge of the BUSY signal to generate an interrupt.

Command	C0	C1
Reset	1	1
Talk	0	1
Testbusy	0	0
Invalid	1	0

Speech Address Buffer/Counter The address counter comprises four 74LS193 ICs which are 4bit binary counters with parallel loading capability (IC4-IC7). The starting address is loaded from the data input lines D0-D7, in two stages. Applying, a low logic level to LDA1 causes the less significant byte of the counter (IC6 & IC7) to be loaded with data setup on input lines D0-D7. Applying a low logic level to LDA0 loads the more significant byte of the counter. Byte address incrementing pulses are derived from IC8 which is programmed as a module 8 counter. lC3b is clocked with pulses generated by VSP on I/O line. IC3b is used to invert the I/O line and as a buffer to provide greater fanout capability. This results in IC8 incrementing its contents on the negative edge of the I/O pulse and consequently keeping track of bitcount, at a byte level, for accessing bit serial speech data. At the commencement of speech, speech data is, output starting with least significant bit of the first speech data byte. Hence, IC8 is cleared every time a new address byte is loaded into the less significant byte of the address counter. The 16bit address counter permits a maximum speech memory capacity of 64K bytes. The total capacity of the memory can be expanded by using extra counter stages, if required. A 64K byte memory will store approximately 600 spoken words.

Speech Data Memory In the circuit shown speech data can be stored in TMS 2516 (16K-bit), TMS 2532 (32K-bit) or TMS 2564 (64Kbit) EPROMs, by wiring an appropriate set of links. Tables 3, 4 and 5 show the links required for each EPROM type and the resulting memory maps. Serial data is derived by the use of a 74LS151, an eight to one line multiplexer. IC10 data input is fed from the data output of EPROMs. The select input of IC10 is obtained from IC8 which maintains a module 8 count which is incremented once, when a single data bit is accessed by the VSP The output of the multiplexer is conveyed through IC2a which is used as a single-bit shiftregister clocked by I/O pulse. The purpose of IC2a is to synchronise serial speech data such that data equested by a particular I/O pulse (see Figure 2) is stored unchanged despite the bit count and the memory address changing as a result of address incrementation.

Table 3: Speech memory address mapping for TMS 2516
Table 4: Speech memory address mapping for TMS 2532
Table 5: Speech memory mapping for TMS 2564

LINKS USED	IC NO.	SPEECH ADDRESS MAP
LK 2	12	0-7FF (0-2047)*
LK 6	13	800-FFF (2048-4095)
LK 7	14	2000-27FF (8192-10239)
LK 9	15	2800-2FFF (10240-12287)
	16	1000-17FF (4096-6143)
	17	1800-1FFF (6144-8191)
	18	3000-37FF (12288-14335)
	19	3800-3FFF (14336-16383)

*Decimal Values

Table 3. Speech memory address mapping for TMS 2516.

LINKS USED	IC NO.	SPEECH ADDRESS MAP
	12	0-FFF (0-4095)*
LK 1	13	1000-1FFF (4096-8191)
LK 6	14	2000-2FFF (8192-12287)
LK 8	15	3000-3FFF (12288-16383)
LK 10	16	4000-4FFF (16384-20479)
	17	5000-5FFF (20480-24575)
	18	6000-6FFF (24576-28671)
	19	7000-7FFF (28672-32767)

*Decimal Values

Table 4. Speech memory address mapping for TMS 2532.

LINKS USED	IC NO.	SPEECH ADDRESS MAP
LK 1	12	0-1FFF (0-8191)*
LK 4	13	8000-9FFF (23768-40959)
LK 9	14	2000-3FFF (8192-16383)
LK 11	15	A000-BFFF (40960149151)
	16	4000-5FFF (16384-24575)
	17	C000-DFFF (49152-57343)
	18	6000-7FFF (24576-32767)
	19	E000-FFFF (57344-65535)

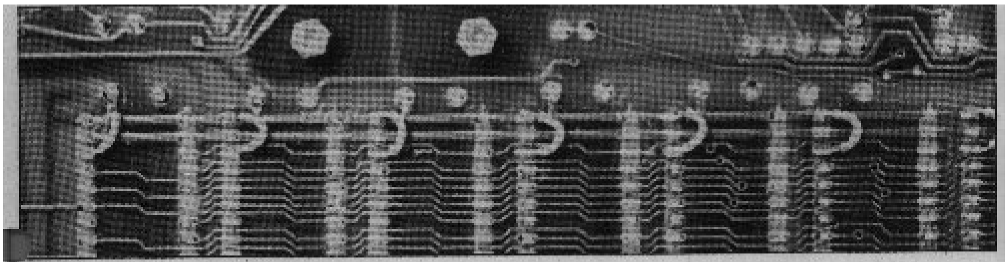
*Decimal Values

Table 5. Speech memory mapping for TMS 2564.

Audio signal Conditioning IC11, a quadoperational amplifier is used to condition the differential audio output of the VSP (SP1 and SP2) into a form suitable for driving a general purpose 8-ohm speaker. IC11a converts the differential pushpull output current into a singleended voltage output. This signal is then low pass filtered by the active filter comprising IC11b to get rid of any harmonic distortion, generated by the 8Khz sampled output from the D to A converter. The thirdstage of the op-amp is used along with transistors TR6-9, to provide power amplification. The amplifier is capable of producing up to 4.5 Watts of audio power into an 8 Ohm speaker. At this power rating, it will be necessary to mount TR8 and TR9 on heatsinks to maintain devices within operating temperature. At reduced power levels, the heat sinking area etched on the PCB should be adequate for normal operation.

Power Supply Requirements Figure 6 shows the distribution of power supplies in the circuit. The negative 5 volt supply is generated on the PCB, by using REG1 (voltage regulator) and tapping on to the negative 12 volts supply. Typical power requirements (for a board fully populated with TMS 2532 EPROMs) are +5V @ 300mA, +12V @ 50mA, -12V @ 50mA without any audio output.

Figure 6: Power supply distribution



Wire links in place for EPROMs supplied.

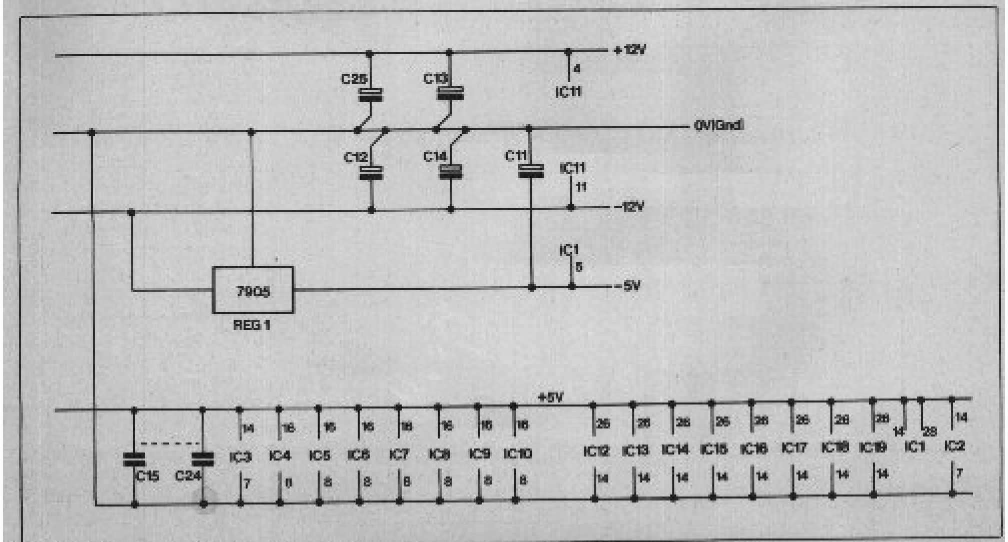


Figure 6. Power supply distribution.

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Speech Data EPROMs Table 7 gives the speech starting addresses for data in the PROMs provided as parts of the kit. EMM1, EMM2, EMM3 and EMM4 should be plugged into IC sockets IC12, IC13, IC14 and IC15 respectively. The links should be connected according to Table 4 (i.e. same as for TMS 2532 EPROMs). In the kit SPST DIL switches are provided for this purpose.

Table 7: E"MM speech data EPROM listing

ADDRESS (Hex)	ADDRESS (Decimal)	WORD
EPROM 1		
0000	0,0	AGAIN
0048	72,0	DOWN
0084	132,0	HELLO
00D0	208,0	MESSAGE
0138	56,1	MISTAKE
0198	152,1	NAME
01CE	206,1	NEED
0222	34,2	PLEASE
0262	98,2	PUT
028C	140,2	REPEAT
02CC	204,2	RIGHT
0324	36,3	THANK
036E	110,3	UP
0388	136,3	WANT
03CE	206,3	'S
03E4	228,3	ALL
041A	26,4	AN
0446	70,4	AND
0484	132,4	ANY
04B4	180,4	ARE
04D0	208,4	AT
04F2	242,4	CAN
0522	34,5	DID
0566	102,5	DO
05A0	160,5	DOES
05FC	252,5	FOR
0634	52,6	FROM
0662	98,6	GOT
069C	156,6	HAVE
06DA	218,6	HOW
0724	36,7	IN
0760	96,7	IS
079C	156,7	IT
07B4	180,7	ME
0800	0,8	MUCH
082A	42,8	MY
0856	86,8	NO
0890	144,8	NOT
08C4	196,8	NOW
0906	6,9	OF
0946	70,9	ON
0970	112,9	OR
099A	154,9	OUT
09D6	214,9	THE(E)
0A08	8,10	THE
0A44	68,10	THERE
0A78	120,10	THIS
0A9E	158,10	USE
0AF6	246,10	WHAT
0B20	32,11	WHEN
0B6C	108,11	WHERE
0BB4	180,11	WILL
0C06	6,12	WITH
0C5A	90,12	WOULD
0C94	148,12	YES
0CC6	198,12	YOU
0CF8	248,12	YOUR
0D2E	46,13	A
0D6C	108,13	B
0DA8	168,13	C
0DEC	236,13	D
0E36	54,14	E
0E60	96,14	F
0E94	148,14	G
0EC4	196,14	H
0EFE	254,14	I
0F34	52,15	J
0F80	128,15	K
EPROM 2		
0000	0,16	L
004C	76,16	M
008A	138,16	N
00C2	194,16	O
00EA	234,16	P
0114	20,17	Q
014C	76,17	R
0178	120,17	S
01A0	160,17	T
01F0	240,17	U
021E	30,18	V
0250	80,18	W
0298	152,18	X
02BE	190,18	Y
0300	0,19	ZED
0346	70,19	ZERO
03A4	164,19	ONE
03F6	246,19	TWO
0430	48,20	THREE
0474	116,20	FOUR
04C2	194,20	FIVE
0510	16,21	SIX
054E	78,21	SEVEN
05A4	164,21	EIGHT
05D4	212,21	NINE
061E	30,22	TEN
0652	82,22	ELEVEN
069A	154,22	TWELVE
06F6	246,22	THIRTEEN
0732	50,23	FOURTEEN
0774	116,23	FIFTEEN
0800	0,24	SIXTEEN
086A	106,24	SEVENTEEN
08C2	194,24	EIGHTEEN
08FC	252,24	NINETEEN
0952	82,25	TWENTY
0986	134,25	THIRTY
09B6	182,25	FORTY
09EC	236,25	FIFTY
0A46	70,26	SIXTY
0A7E	126,26	SEVENTY
0AC4	196,26	EIGHTY
0AF0	240,26	NINETY
0B58	88,27	HUNDRED
0BC2	194,27	THOUSAND
0C3E	62,28	EQUAL
0C94	148,28	NUMBER
0D04	4,29	PERCENT
0D54	84,29	AMPS
0D94	148,29	DEGREES
0DF4	244,29	FARAD
0E62	98,30	FREQUENCY
0ECE	206,30	HENRY
0F18	24,31	HERTZ
0F66	102,31	HOURS
EPROM 3		
0000	0,32	MEGA
005E	94,32	MICRO
00D2	210,32	MILLI
010A	10,33	MINUS
0172	114,33	OHMS
01C6	198,33	PLUS
01FA	250,33	POINT
023C	60,34	POWER
0282	130,34	SECONDS
02EA	234,34	TEMPERATURE
0362	98,35	TIME
03AC	172,35	READY
03F0	240,35	SWITCH
043E	62,36	CONTROL
04A2	162,36	WARNING
04EC	236,36	OFF
0530	48,37	CHECK
0566	102,37	BUTTON
05B6	182,37	TELEPHONE
0608	8,38	BUSY
0656	86,38	INVALID
06F6	246,38	MONDAY
0752	82,39	TUESDAY
0800	0,40	WEDNESDAY
0872	114,40	THURSDAY
08D2	210,40	FRIDAY
0938	56,41	SATURDAY
0984	132,41	SUNDAY
09DE	222,41	GOODBYE
0A36	54,42	DATE
0A6A	106,42	LEFT
0A98	152,42	CHANGE
0ADE	222,42	DIRECTION
0B5C	92,43	ENTER
0BA6	168,43	FAST
0C00	0,44	SLOW
0C48	72,44	GO
0C9C	156,44	STOP
0CEA	234,44	HIGH
0D46	70,45	LOW
0D9A	154,45	MOVE
0E10	16,46	RANGE
0E7E	126,46	EXIT
0EBE	190,46	CARDS
0F10	16,47	ATTACK
0F4C	76,47	DESTROY
EPROM 4		
0000	0,48	START
003C	60,48	INSERT
0096	150,48	LOSE
00D0	208,48	WIN
010C	12,49	TRY
0140	64,49	O'CLOCK
0196	150,49	OVER
01D2	210,49	UNDER
0218	24,50	WAIT
0248	72,50	ADDRESS
0294	148,50	LINE
0312	18,51	OPERATOR
037A	122,51	COMPUTER
03E4	228,51	CALL
0428	40,52	INITIALISE
04BC	188,52	INTRUDER
051E	30,53	TEST
0574	116,53	MANUAL
05E8	232,53	AUTOMATIC
064A	74,54	PROCESSING
06C4	196,54	CLOCK
06F4	244,54	GAMBLE
0762	98,55	HOLD
0800	0,56	SHUFFLE
084E	78,56	HARDLUCK
08C8	200,56	ALARM SOUND
08EA	234,56	SHORT TONE
08FE	254,56	PLEASING TONE
0918	24,57	PIE
094C	76,57	PASS
09C2	194,57	POSITION
0A4A	74,58	PUSH
0A80	128,58	PRESENT
0AD6	214,58	GREEN
0B14	20,59	RED
0B4C	76,59	YELLOW

Table 7. E&MM speech data EPROM listing.

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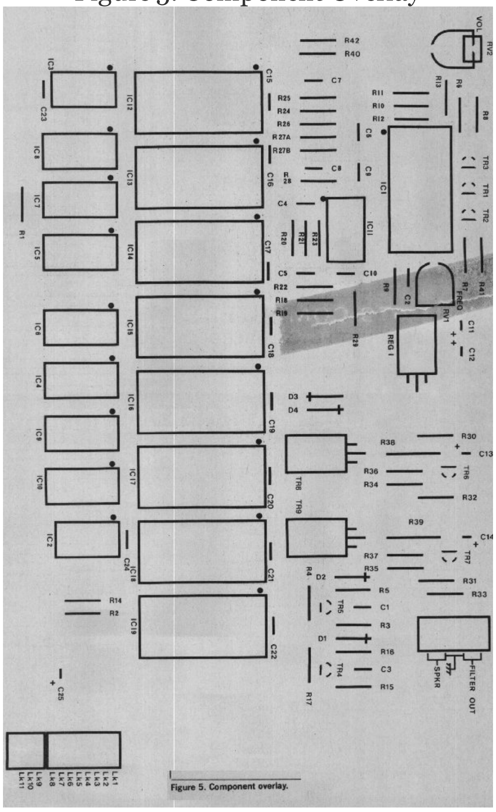
Construction and Setting Up

Figure 5 shows the component overlay for the circuit. The first step is to fit all the necessary links between the two sides of the PCB (using Track pins or small lengths of wire). Care should be taken when soldering on this board as the tracks are fine and often very close together. The resistors and capacitors can then be fitted, followed by the diodes, soldering both sides where necessary. Next, make all the IC sockets using Soldercon connectors and again solder to both sides of the PCB where necessary. Having completed these stages you can fit the transistors, the voltage regulator (REG1) and IC11.The powertransistors (TR8, TR9) and the negative 5 volt regulator should be positioned flat as shown in Figure 5 and bolted on to the PCB to achieve good thermal dissipation.

Figure 5: Component Overlay



Before you plug in any more ICs, connect a low impedance speaker and power up the (connection details are shown in Table 6). Check the supply currents and voltages (the current should be approximately 50mA on +12V lines and negligible on +5V line). Next, check the amplifier is operating. If all is well can proceed and fit the rest of the components. The pin numbers given in circuit diagram are correct for the TMS 2564 only. TMS 2532 and TMS 2516 ICs have 24 pins compared with 28 pins for the 2564. The signal lines match when the lower 24 pins of the 28 pin configuration are used (i.e. pin numbers 1, 2, 27 & 28 are not used).

Table 6: Edge connector details

PIN	SIGNAL	PIN	SIGNAL
20	D0	17	GND
22	D1	15	GND
14	D2	13	GND
16	D3	11	GND
18	D4	9	GND
10	D5	39	GND
12	D6	37	GND
24	D7	35	GND
26	LDA0	33	GND
28	LDA1	31	GND
32	C0	29	GND
34	C1	27	GND
36	CCLK	25	GND
38	BUSY	23	GND
1	+12V	21	GND
2	-12V	19	GND
3	+5V	5	GND

Table 6. Edge connector detail.

Note: When using 24-pin p packages you must link pin 28 to pin 26 on ICs 12-19 (see photo) For correct speed of operation the TMS 5100 internal clock frequency should be adjusted with RV1 to obtain a square wave of period 6.25us (a frequency of 160KHz) at ROM CLK (pin 3) of IC1. The correct adjustment is nominally midway on RV1. If instruments for adjustment are not available, good results can be obtained by listening to the speech output and making the adjustment such that the output sounds 'normal'.

Photo: Wire links in place for EPROM's supplied
not available

Care should be taken in handling the TMS 5100 which can be damaged by static discharges. The kit of parts does not contain an edge connector. The RS467-425 20-way, double edge connector is suitable and instead of Veropins for soldering the speaker connections, the screw connector socket (RS423-762) can be used (both available from Radio Spares). A suitable Power Supply circuit diagram for the WORDMAKER is shown in Figure 11.

Figure 11: Suggested power supply

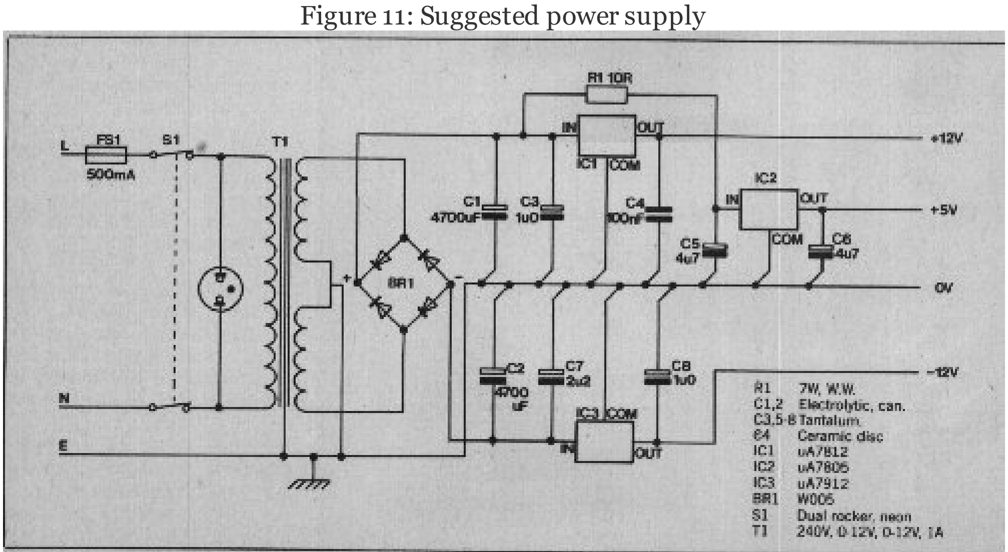


Figure 11. Suggested power supply circuit diagram.

Now you know all about the E&MM WORDMAKER but is it any use to you? The all-important question is 'Will it interface to my microcomputer?' Well, here is a simple guide to give you some idea. List 1 contains all the popular systems which can be used with available modules. List 2 contains all the popular microcomputers which will drive the WORDMAKER if a simple dedicated interface is used such as the one shown.

LIST 1

Sharp MZ-80K	with parallel I/O card and expansion unit
Nascom 1 & 2	as standard
Apple/ITT 2020	with parallel I/O card
Commodore Pet	with parallel I/O expansion
Atari 400 & 800	with parallel I/O expansion
Tangerine Micron	as standard
Acorn	as standard
Video Genie	with parallel I/O expansion

LIST 2

Microcomputer	Addressing mode
Sharp MZ-80K	I/O mapped
Tandy TRS 80	I/O mapped
Sinclair Zx80/81	I/O mapped
Apple/ITT 2020	memory mapped
Commondore Pet	memory mapped
Atari 400 & 800	memory mapped
UK 101	memory mapped
OHIO Superboard	memory mapped

Using the Wordmaker

Communication with the VSP card is carried out through two ports; one to supply the address of the word defining data in the V/S ROM, and the other to set the various control functions. There are two preset potentiometers on the card; RV1 controls the spead and pitch of the voice; RV2 controls the volume of the onboard amplifier. All the connections on the board are TTL compatible for easy interfacing (see Figures 9 and 10).

Figure 9: Connection to a standard PIO/PIA port

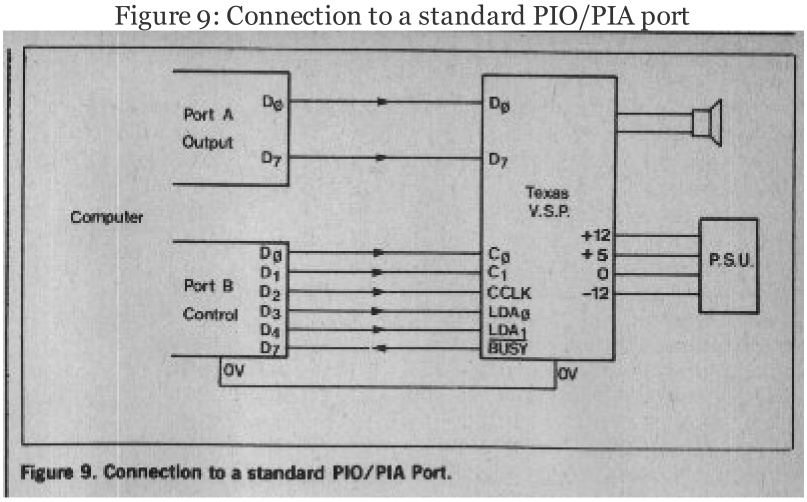


Figure 10: Purpose-built interface (memory mapped or I/O addressed

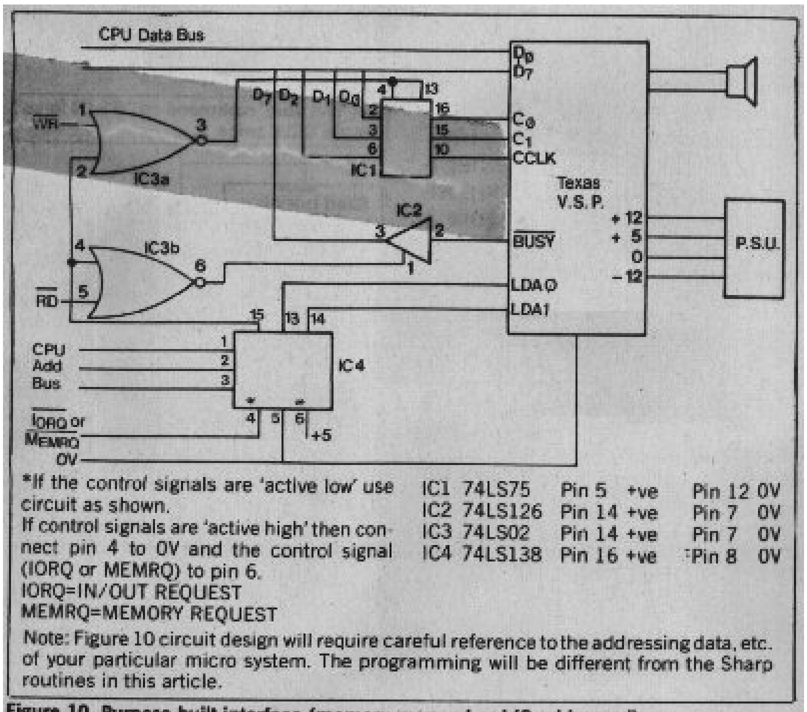


Figure 10. Purpose-built interface (memory mapped or I/O addressed).

The VSP card is very simple to use and the flowcharts in Figure 7 show the sequence of operations. Figure 8 shows the sequence of commands and the relevant timing. On 'power up' the card must be initialised bysettirig C0 and C1 to 'RESET' (see Table 2), toggling CCLK 3 times then setting C0 and C1 to 'TEST BUSY' and toggling CCLK a further 3 times. The card is then ready to talk to you. The flowchart in Figure 7(a) also shows a 'dummy test talk' command can be executed in order to avoid an audible click that may be generated prior to commencement of speech. To make it speak the address of the word is written to the card.

Figure 7: Flowchart

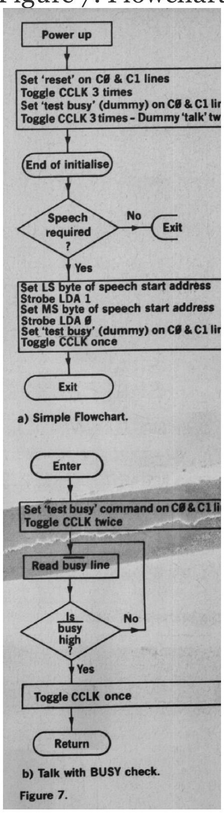


Figure 8: VSP interface control signal timing

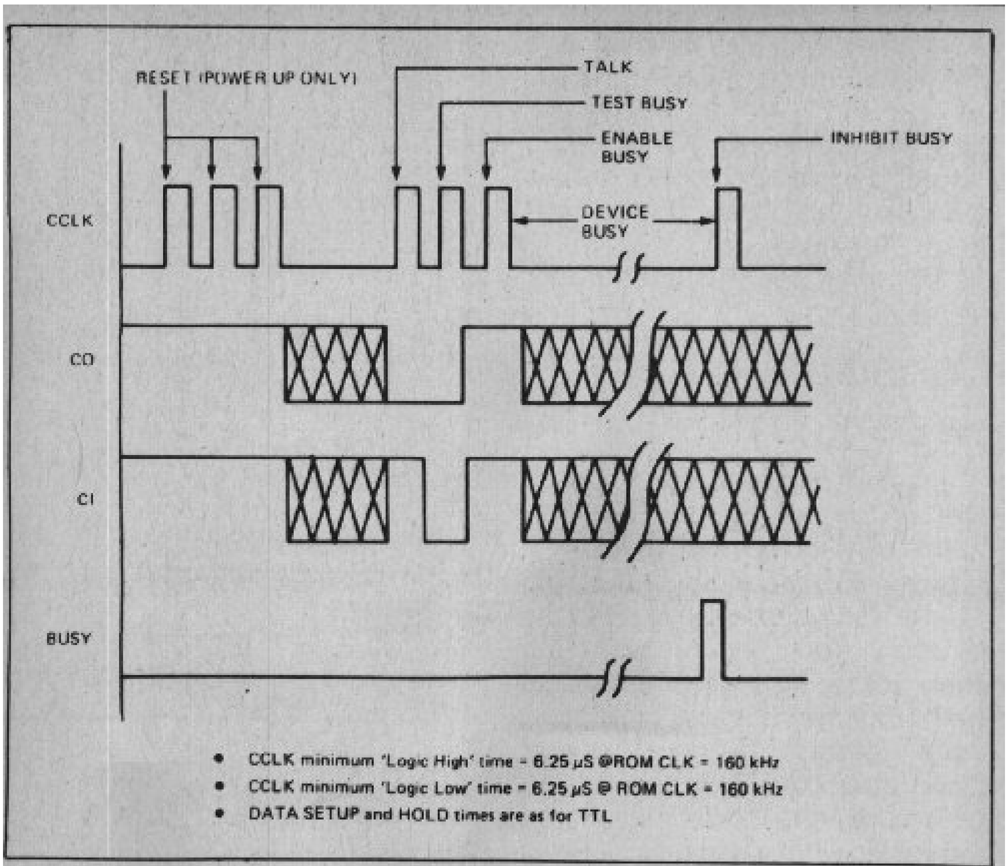
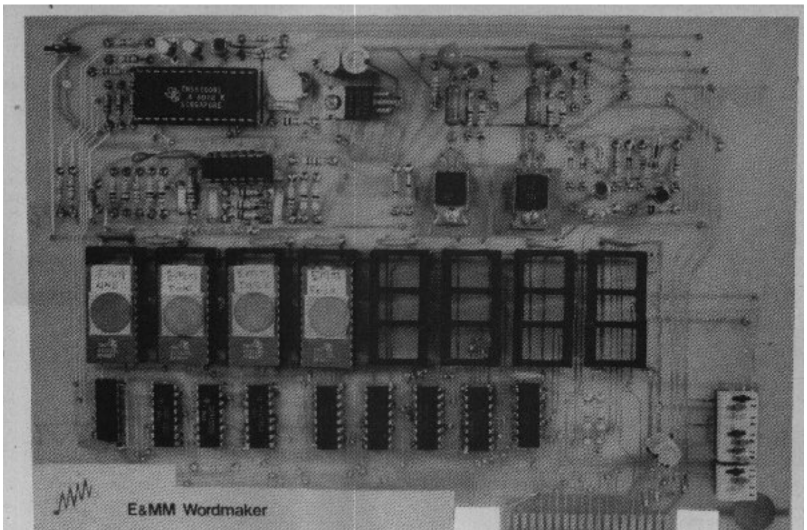


Figure 8. VSP Interface control signal timing.

The two address bytes are latched into the VSP card by taking LDA1 (for LS byte) and LDA0 (for MS byte) low for at least 6.25us (at an oscillator frequency of 640kHz). It is important to note that the LS byte must be loaded first. Having set up the address all we need to do now is send the 'TALK' command on C0 and C1 and toggle CCLK once. Then: Hey Presto, it speaks! If any problems are encountered at this point, a logic probe will be useful for checking that the control and data input lines are providing the correct 'high'/'Iow' signals via the board connector to the EPROMs and associated logic ICs. Resistor values for R40, R41 R42 may need changing in order to get the right 'pullup'.

Wordmaker circuit board



WORDMAKER circuit board.

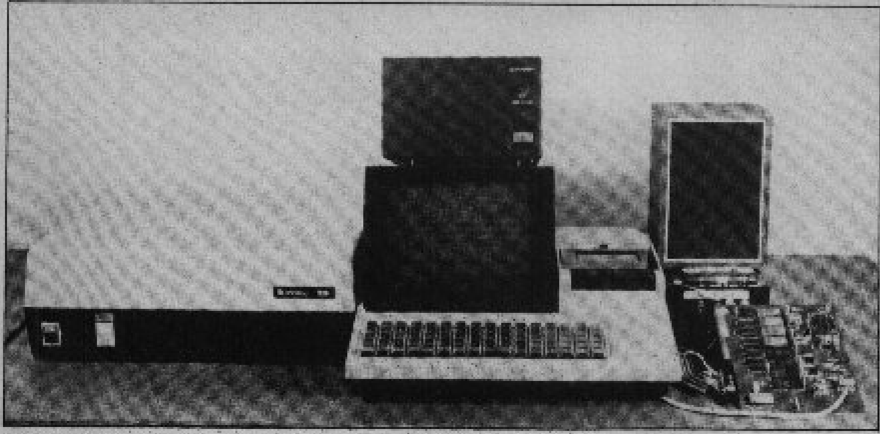
If you are using the VSP card with a computer system it wi probably become necessary some stage to be able to test whe one word has finished so you ca start another. If you try and start word while the VSP is speaking, will miss the end of the first word and say the next - or it might just stop altogether. Using the 'TEST BUSY' command it is possible to monitor the BUSY line. This done by setting the 'TEST BUSY' command on C0 and C1 and toggling CCLK twice, then reading the BUSY line. When BUSY goes high you toggle CCLK once more and then initiate the next talk cycle. The BUSY line output (connector pin 38) need not be connected when first testing the board for correct speech opera tion (e.g. using Test Program 1)

Some Simple Programs

These programs are written BASIC to run on the Shar MZ-80K. The port is assumed to be addressed I/O. If you wish to use a memory-mapped syster replace all output statement with 'pokes' and input statement with 'peeks'. The programs ar written as subroutines to aIIow them to be easily incorporate into existing BASIC program (see Subroutines). During the 'Initialise' subroutine, you will need to specify the port address. On the Sharp this is simply two numbers, say 2 and 3.

Test Program 1: By entering the word start address in decimal when prompted, the VSP card will say the word. WL=LS byte, WH=MS byte. This program is a continual loop and to stop use escape', 'break' or 'control C' command. **Test Program 2:** By entering a string of word start addresses in the DATA line as follows: WL1, WH1, WL2, WH2 ...., the VSP card can be made to speak the entered sentence or phrase. If you use the data list (lines 35-62) the WORDMAKER speaks the whole word library available in correct EPROM order (see Table 7). Note that the 'decimal' Address has the correct numbers for operation instead of a straightforward Hex conversion. **Test Program 3:** This program, based on Test Programs 1 and 2, gives some sample sentences and tones which are recorded on our demonstration cassette No.2. Pauses of varying lengths are easily made by inserting a FOR / NEXT loop at line 28 as shown. Some idea of the musical potential, using varying pitch/clock rates by adjusting RV1 (this can be increased to 100k for greater range), is also given. Exciting possibilities are evident here.

Program listings 1



Using the WORDMAKER with the Sharp MZ-80K.

```
1 REM E&MM WORDMAKER SHARP MZ80-K
2 REM INITIALISE PORTS
3 REM A=OUTPUT(D0-D7),B=CONTROL(D0=LDA0,D1=LDA1,D2=C0,D3=C1,D4=CCLK)
4 REM 1 Input BUSY also required - use D7 on port B,or an INPUT PORT.
5 REM PA=ADDRESS of PORT A data        PB=ADDRESS of PORT B data
6 INPUT"PORT A ADDRESS";PA
7 INPUT"PORT B ADDRESS";PB
8 FORI=1TO3:A=27:OUT#PB,A:A=A+4:OUT#PB,A:NEXTI
9 FORJ=1TO3:A=24:OUT#PB,A:A=A+4:OUT#PB,A:NEXTJ
10 OUT#PB,24:WL=0:WH=0:GOSUB12:GOSUB12
11 RETURN


12 REM TALK SUBROUTINE
13 OUT#PA,WL:OUT#PB,0:OUT#PB,24
14 OUT#PA,WH:OUT#PB,16:OUT#PB,24
15 OUT#PB,30:OUT#PB,26:OUT#PB,24:RETURN


16 REM SUBROUTINE WITH BUSY CHECK
17 FORI=1TO2:A=28:OUT#PB,A:A=A-4:OUT#PB,A:NEXTI
18 INP#PA,B
19 IFB<128THEN18
20 OUT#PB,28:OUT#PB,24:RETURN
```

Subroutines.

```
21 REM TEST PROGRAM ONE
22 GOSUB 2
23 INPUT"WL";WL
24 INPUT"WH";WH
25 GOSUB12
26 GOTO 23
```

Test Program 1.

```
27 REM TEST TWO
28 PRINT"£"
29 GOSUB2
30 READ WL
31 READ WH
32 GOSUB17
33 GOSUB12
34 GOTO30
35 REM EPROM 1 WORDS:-
36 DATA 0,0,72,0,132,0,200,0,56,1,152,1,206,1,34,2,90,2,140,2,204,2,36,3
37 DATA 110,3,136,3,206,3,228,3,26,4,70,4,132,4,180,4,208,4,242,4,34,5
38 DATA 102,5,160,5,252,5,52,6,98,6,156,6,218,6,36,7,96,7,156,7,180,7
39 DATA 0,8,42,8,86,8,144,8,196,8,6,9,70,9,112,9,154,9,214,9,0,10,68,10
40 DATA 120,10,150,10,246,10,32,11,100,11,180,11,6,12,90,12,148,12,190,12
41 DATA 248,12,46,13,108,13,160,13,236,13,54,14,96,14,148,14,196,14
42 DATA 254,14,52,15,128,15
43 REM EPROM 2 WORDS:-
44 DATA 0,16,76,16,138,16,194,16,234,16,20,17,76,17,128,17,160,17,240,17
45 DATA 30,18,80,18,152,18,190,18,0,19,70,19,164,19,246,19,40,20,116,20
46 DATA 194,20,16,21,78,21,164,21,212,21,30,22,82,22,134,22,246,22,50,23
47 DATA 116,23,0,24,106,24,194,24,252,24,82,25,134,25,182,25,236,25,70,26
48 DATA 126,26,196,26,240,26,80,27,194,27,62,28,148,28,4,29,84,29,140,29
49 DATA 244,29,98,30,206,30,24,31,182,31
50 REM EPROM 3 WORDS:-
51 DATA 0,32,94,32,210,32,10,33,114,33,198,33,250,33,60,34,130,34,234,34
52 DATA 98,35,172,35,240,35,62,36,162,36,236,36,48,37,102,37,182,37
53 DATA 8,38,86,38
54 DATA 246,38,82,39,0,40,114,40,210,40,56,41,132,41,222,41,54,42,106,42
55 DATA 152,42,222,42,92,43,166,43,0,44,72,44,156,44,234,44,70,45,154,45
56 DATA 16,46,126,46,190,46,16,47,76,47
57 REM EPROM 4 WORDS:-
58 DATA 0,48,60,48,150,48,200,48,12,49,64,49,150,49,210,49,24,50,72,50
59 DATA 140,50,18,51,122,51,228,51,40,52,180,52,30,53,116,53,232,53
60 DATA 74,54,196,54,244,54,98,55,0,56,78,56,200,56,234,56,254,56,24,57
61 DATA 76,57,194,57,74,58,120,58,214,58,20,59,76,59
62 REM END OF EPROMS 1-4 WORD DATA
63 COPYRIGHT E&MM 1981
```

Test Program 2 (Including complete EPROM data).

```
1 REM E&MM WORDMAKER SHARP MZ80-K
2 REM INITIALISE PORTS
3 REM A=OUTPUT(D0-D7),B=CONTROL(D0= LDA0,D1=LDA1,D2=C0,D3=C1,D4=CCLK)
4 REM 1 Input BUSY also required -  use D7 on port B,or an INPUT PORT.
5 REM PA=ADDRESS of PORT A data         PB=ADDRESS of PORT B data
6 PRINT"£"
7 INPUT"PORT A ADDRESS";PA
8 INPUT"PORT B ADDRESS";PB
9 GOSUB22
10 FORI=1TO3:A=27:OUT#PB,A:A=A+4:OUT#PB,A:NEXTI
11 FORJ=1TO3:A=24:OUT#PB,A:A=A+4:OUT#PB,A:NEXTJ
12 OUT#PB,24:WL=0:WH=0:GOSUB14:GOSUB14
13 RETURN
14 OUT#PA,WL:OUT#PB,8:OUT#PB,24
15 OUT#PA,WH:OUT#PB,16:OUT#PB,24
16 OUT#PB,30:OUT#PB,26:OUT#PB,24:RETURN
17 REM SUBROUTINE WITH BUSY CHECK
18 FORI=1TO2:A=28:OUT#PB,A:A=A-4:OUT#PB,A:NEXTI
19 INP#PA,B
20 IFB<128THEN19
21 OUT#PB,28:OUT#PB,24:RETURN
22 REM TEST THREE/SPEECH
23 PRINT"£"
24 PRINT"±±±±±±±E&MM WORDMAKER SPEECH EXAMPLES"
25 GOSUB10
26 READ WL
27 READ WH
28 IFWL=0THENIFWH=1THENFORD=1TO1000:NEXTD:GOTO26
29 GOSUB18
30 GOSUB14
31 GOTO26
32 DATA 8,10,98,35,96,7,196,8,78,21,64,49
33 DATA 0,1,162,36,0,1,200,56,162,36,0,1,188,52,70,9,0,40,0,1
34 DATA 254,56,254,56,34,2,48,37,70,4,40,52,214,9,94,32,122,51,0,1
35 DATA 132,0,0,1,8,10,234,34,96,7,234,44,208,4,240,26,78,21,148,29,234,56
36 DATA 0,1,36,3,198,12,0,1,246,10,180,11,248,12,208,0,108,13,246,19
37 DATA 206,30,70,9,56,41,34,2,0,1,0,1,156,7,96,7,120,10,0,1
38 DATA 240,35,236,36,8,10,60,34,250,33,206,3,70,4,228,51,180,7,70,9
39 DATA 8,10,182,37,254,56,254,56,42,8,148,28,96,7,48,20,48,20,164,21
40 DATA 164,21,78,21,164,21,234,56,234,56,222,41,0,1
41 DATA 234,56,254,56,18,51,0,1,240,35,62,36,212,21,208,4,70,19,0,1
42 DATA 36,3,206,3,0,1
43 REM PROGRAM compiled by Glenn Rogers and Mike Beecher
44 REM COPYRIGHT E&MM 1981
```

Test Program 3.

Parts list

PARTS LIST

Resistors — all 5% ⅓W carbon unless specified

R1,2,3,5,6,7,8,14, 15,16,40,41,42	4k7	(13 off)
R4,9,10,11,12,17,20, 21,22,23,25,27A,27B	10k	(13 off)
R13	22k	
R18,19	47R	(2 off)
R26,29	6k8	(2 off)
R28	1k	
R24	12k	
R30,31	8k2	(2 off)
R32,33	2k2	(2 off)
R34,35	82R	(2 off)
R36,37	22R	(2 off)
R38,39	2R2 3 Watt wire wound	(2 off)
RV1	50k cermet preset	
RV2	22k vert. S-min preset	

Note: R27=R27A + R27B

Capacitors

C1,3	100pF polystyrene	(2 off)
C2	68pF polystyrene	
C4,5,8	1nF polystyrene	(3 off)
C6,7	10nF disc ceramic (2 off)	
C9,15-24	100nF disc ceramic	(11 off)
C10	2n2 polycarbonate	
C11,12,25	47uF 25v p.c. electrolytic	(3 off)
C13,14	47uF 16v tantalum	(2 off)

Semiconductors

TR1-5	BC212	(5 off)
TR6	BC183	
TR7	BC213	
TR8	TIP31	
TR9	TIP32	
IC1	TMS5100	
IC2	74LS74	
IC3	74LS04	
IC4-8	74LS193	(5 off)
IC9	74LS138	
IC10	74LS151	
IC11	TL084	
IC12-15	2532 speech coded EPROM	(EMM1-4)
Reg 1	7905	
D1-4	1N4148	(4 off)

Miscellaneous

	Soldercons	
	Veropins	
	Track pins	
LK1-8	Octal SPST DIL switch	
LK9-12	Dual SPST DIL switch	(2 off)

We hope you will find the simple programs helpful in your investigation into the world of talking computers and that you wont spend too many hours talking to your computer as opposed to your family or friends!E"MM

RDjan2001